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10/826,375	04/19/2004	Shahar Atir	P-6343-US	9730

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
09/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PUSDKT@EM-LG.COM

Office Action Summary	Application No.	Applicant(s)	
	10/826,375	ATIR ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/03/2009 (AF and RCE)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/19/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Amendments and RCE filed on 08/03/2009. Claims 1-11 are examined. Claims 12-17 have been withdrawn. Applicant is requested to cancel claims 12-17 in the next response.

Claim Rejections - 35 USC § 112

2. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

Claim 1 lines 2-3 recites limitation "sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path including a common sense amplifier", which is the source-side read operation described in FIG. 2A and paragraph [0023]-[0025] of the present invention. As mentioned in paragraph [0025], in the source-side read operation, the reading node [i.e. common node] may act as the **source** of the cells. If so, the other terminals of the cells may act as the drains of the cells, and the bit lines coupled to the drains of the cells are so called **drain side bit lines**.

Therefore, the claimed limitation "wherein sensing includes applying ..... similar voltage to the **source side bit lines** of the cells", in claim 1 line 4-5, is conflicting with the above interpretation.

For the purpose of examination, Examiner assumes "the source side bit lines of the cells" are the drain side bit lines of the cells.

Claim 1 line 5 recites limitation "the cells", it is not clear whether the cells are the memory cells of the whole array claimed in line 1, or the adjacent memory cells in line 2.

For the purpose of examination, Examiner assumes "the cells" are the adjacent memory cells.

Claim 2:

In claim 2 line 2, is "a sense amplifier" different from "a common sense amplifier" in claim 1 line 3?

For the purpose of examination, Examiner interprets "a sense amplifier" in claim 2 line 2 as --the common sense amplifier--.

Claims 6 and 11:

Claim 1 lines 2-3 recites limitation "sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path including a common sense amplifier", which is the source-side read operation described in FIG. 2A and paragraph [0023]-[0025] of the present invention. As described, in the source-side read operation, common bit line BL_4 is the read node and coupled to a common sense amplifier. The outside bit lines BL_3 and BL_5 coupled to a voltage source.

Claim 6 lines 2-3 later recites the method including "coupling said [common] sense amplifier to bit lines of said adjacent cells that are not shared by said adjacent cells". There appears the bit lines of the adjacent cells that are not shared by said adjacent cells are bit line BL_3 and BL_5 of FIG. 2A.

How is that possible for the [common] sense amplifier is first coupled to the shared bit line, e.g. bit line BL_4 of FIG. 2A, as claimed in claim 1 lines 2-3, then later coupled to the unshared bit lines, e.g. bit lines BL_3 and BL_5 of FIG. 2A, as claimed in claim 6 lines 2-3?

Same rejection and interpretation applied for claim 11.

Claims 6 and 11 are temporary withdrawn from consideration due to the above 112 rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,831,892 to Thewes et al. ("Thewes").

Regarding independent claim 1, Thewes discloses, in FIG. 1, a method of reading data in a virtual ground array of memory cells comprising:

- sensing substantially simultaneously a state of adjacent memory cells, wherein a bit stored in each cell of said adjacent memory cells through at least a partially shared sensing path including a common sense amplifier (FIG. 1: evaluation circuit AWS, also see col. 1 ll. 6-12), wherein sensing includes applying a first voltage to a common word line (FIG. 1: switch $S'_{k,vwl}$ of the cells to be read out are closed, coupled the selected word line to V_{wl} of 5V, see col. 4 ll. 6-13).

Thewes further discloses the two adjacent memory cells might store different data (see col. 4 ll. 22-55), which is the reason why the drain side bit lines of the adjacent memory cells are applied with two different lower potentials Vm and Vgnd.

The present invention requires the two adjacent memory cells are in identical state, which falls into category (a) and (d) taught in Thewes (see col. 4 ll. 22-55). As seen in Thewes, the potential difference between Vm and Vgnd applied to drain side bit lines does not make any different during the sensing operation of two adjacent memory cells stored same data.

Therefore, it would have been obvious to one with ordinary skill in the art to apply substantially similar voltage to both drain side bit lines during the sensing operation of two adjacent memory cells stored same data, since it have been held that adjustability, where needed, involves only routine skill in the art (*In re Steven*).

Regarding dependent claim 2, Thewes further discloses wherein said sensing substantially simultaneously comprises:

- coupling a sensing circuit to a first source/drain terminal of each cell of said adjacent memory cells (FIG. 1: coupling evaluation circuit AWS to bit line BLn);
- setting a voltage at a second drain/source terminal of each cell of said adjacent cells to a read level (FIG. 4: setting bit line BLn-1 to ground and bit line BLn to Vvm); and
- sensing in a reading direction the state of said adjacent cells (see col. 4 ll. 19-55).

Regarding dependent claims 3-5 and 10, Thewes further discloses wherein adjacent cells share a word line WL_k, an inside bit line BL_n, the evaluation circuit AWS coupled to the inside/shared bit line BLn,

Regarding dependent claim 7, Thewes inherently discloses wherein any one of said memory cells stores at least one bit in said charge trapping region (because the memory cells in Thewes are EPROM cells, see col. 3 ll. 6-15).

Regarding dependent claim 8, Thewes discloses wherein said adjacent cells are sense with substantially identical current (because they both have the same sense current).

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thewes in view of U.S. Patent No. 6,975,536 to Maayan et al. ("Maayan").

Thewes discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitation as set forth in claim 9.

Regarding dependent claim 9, Maayan discloses, in FIG. 1, a virtual ground memory device comprising nitride read only memory (NROM) cells

Since Thewes and Maayan are all from the same field of endeavor, the purpose disclosed by Maayan would have been recognized in the pertinent art of Thewes.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the method of reading disclosed in Thewes for the NROM memory device in Maayan in order to shortening the duration of read time (see col. 1 ll. 6-11).

Response to Arguments

6. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

35 U.S.C. 112 Rejections

In response to Applicant's argument regarding 112 rejection, Examiner understands the concept of interchangeable source/drain operations. However, Examiner finds it difficult to understand how it is possible for the common sense amplifier, which is first coupled to a shared bit line as claimed in claim 1, lines 2-3, then is later coupled to unshared bit lines as claimed in claim 6, lines 2-3.

Examiner agrees paragraph [0024] of the present invention supports the claimed limitation of a common sense amplifier coupled to a shared bit line BL_4, but it does not support limitations of common sense amplifier coupled to unshared bit lines BL_3 and BL_5 of the same embodiment. In fact, paragraph [0024] of the specification describes the unshared bit lines BL_3 and BL_5 are coupled to a voltage source.

Assuming arguendo there is a common sense amplifier coupled to ALL bit lines of the memory array, which would meet recited limitations in both claims 1 and 6, then there raises another question of how it is possible for unshared bit line BL_3 and BL_5 coupled to a voltage source as described in paragraph [0024] of specification, and also coupled to a common sense amplifier as claimed in claim 6 during a read operation?

Examiner was unsuccessful in attempt to contact Applicant on 8/26/2009 to clarify the above 112 issues.

35 U.S.C. 102 Rejections

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 8, 2009

/VanThu Nguyen/
Primary Examiner
Art Unit 2824